ABSTRACT

Electronic design automation tool specifies an architecture at a system level and its component (which include intellectual property (IP) cores like embedded processors, arithmetic logic units (ALU), multipliers, dividers, embedded memory element, programmable logic cells, etc.); specifies IP-cores and their interface; and understands IP-cores and functions via their interface. Further, techniques are provided for modeling the timing behavior of a function or functional block without drawing a timing diagram; understanding the interface behavior of a function block which captures the timing waveforms; specifying virtual functions which are built using basic functional units and their timing behavior; parsing and creating an internal graphical form for analyzing a specification for compilation; matching the components in the architecture specification and their instantiation to map the computations in the input graph produced from an application; and mapping the specification onto the *target's* components.